



J23-83

**PATENT NUMBER and
ISSUE DATE****U.S. UTILITY Patent Application**

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10043276	01/14/2002	438	1	2812	JML

****APPLICANTS:** Nakatani Goro; Sakamoto Tatsuya;****CONTINUING DATA VERIFIED:** JML
none**BEST AVAILABLE COPY****** FOREIGN APPLICATIONS VERIFIED:** JML
JAPAN 2001-6581 01/15/2001

FO-17B	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	040894-5755	
Verified and Acknowledged Examiner's initials	JML		
TITLE : Semiconductor device and method for manufacturing the same			
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Draw.	Fig. Draw.
<input type="checkbox"/> TERMINAL		Application Examiner	
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